WHAT IS CLAIMED IS:

1. An apparatus for adaptive modulation, comprising:

a one-bit modulator for generating a binary output signal from an analog input signal; and

a multi-bit adapter for generating a scaling signal for scaling a step-size of the modulator.

2. The apparatus of claim 1, wherein the adapter includes a companded differential pulse code modulator (DPCM).

3. The apparatus of claim 2, wherein the adapter includes a logarithm term block for companding an absolute value of a filtered error signal, the companded DPCM for modulating an output of the logarithm term block, and an exponential term block for expanding an output of the companded DPCM.

4. The apparatus of claim 1, wherein the modulator comprises:

a summing junction for comparing an analog input signal x(n) to an encoding signal v(n) to generate an error signal e(n) representing a difference between the analog input signal x(n) and the encoding signal v(n);

a filter for filtering the error signal e(n) to generate a signal p(n);

a quantizer for converting the signal p(n) into a binary output signal y(n);

a multiplier for multiplying the analog output signal y(n) by a scaling signal d(n) output by the adapter to generate an encoding signal v(n); and

a delay for the dealying the encoding signal v(n) to generate a delayed encoding signal v(n-1).

5. The apparatus of claim 4, wherein the adapter produces both the scaling signal d(n), which is an approximation of the absolute value of the signal p(n), and a binary sequence signal q(n) from which the scaling signal d(n) can be re-generated.

6. The apparatus of claim 1, wherein the adapter is used in an adaptive sigma-delta modulator.

7. The apparatus of claim 1, wherein the adapter is used in an adaptive delta modulator.

8. The apparatus of claim 1, wherein the adapter is used as a companded delta modulator.

9. An apparatus for adaptive demodulation, comprising:

a multi-bit adapter for receiving a binary sequence signal q(n) from an adapter of an adaptive modulation apparatus and for generating a scaling signal d(n) in response thereto;

a multiplier for multiplying a binary output signal y(n) received from a modulator of the adaptive modulation apparatus by the scaling signal d(n) to generate an encoding signal v(n); and

a low-pass filter for receiving the encoding signal v(n) and for generating a signal $\hat{x}(n)$, which is a re-creation of an analog input signal x(n) to the modulator of the adaptive modulation apparatus.

10. The apparatus of claim 9, wherein the adapter includes a companded differential pulse code modulator (DPCM).

11. The apparatus of claim 10, wherein the adapter includes a logarithm term block for companding an absolute value of a filtered error signal, the companded DPCM for modulating an output of the logarithm term block, and an exponential term block for expanding an output of the companded DPCM.

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12. The apparatus of claim 9, wherein the adapter is used in an adaptive sigma-delta modulator.

13. The apparatus of claim 9, wherein the adapter is used in an adaptive
10 delta modulator.

14. The apparatus of claim 9, wherein the adapter is used as a companded delta modulator.